



TSMC-03-627

April 30, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/807,081 03/23/04 |
Hung-Wei Chen et al.
METHOD FOR REDUCING A SHORT CHANNEL
EFFECT FOR NMOS DEVICES IN SOI
CIRCUITS
| _____ |

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on May 4, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

Stephen B. Ackerman 5/4/04

U.S. Patent 5,468,657 to Hsu, "Nitridation of SIMOS Buried Oxide," discloses a method for improving the electrical isolation between surface regions and underlying support regions in SIMOX buried oxide wafers.

U.S. Patent 6,613,678 to Sakaguchi et al., "Process for Manufacturing a Semiconductor Substrate as Well as a Semiconductor Thin Film, and Multilayer Structure," discloses a process for manufacturing a semiconductor substrate as well as a semiconductor thin film.

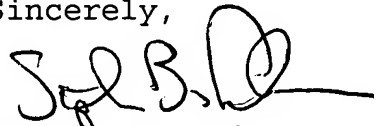
U.S. Patent 6,410,938 to Xiang, "Semiconductor-on-Insulator Device with Nitrided Buried Oxide and Method of Fabricating," discloses methods of preventing dopant depletion in active regions of semiconductor devices.

U.S. Patent 5,910,672 to Iwamatsu et al., "Semiconductor Device and Method of Manufacturing the Same," discloses a semiconductor device with a SOI structure and a method of manufacturing the same, preventing deterioration in and making improvement in device characteristics.

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U.S. Patent 5,656,537 to Iwamatsu et al., "Method of Manufacturing a Semiconductor Device Having SOI Structure," discusses a method of manufacturing a semiconductor device having an SOI (Semiconductor On Insulator) structure.

Sincerely,

A handwritten signature in black ink, appearing to read "S.B. Ackerman", with a long horizontal flourish extending to the right.

Stephen B. Ackerman,
Reg. No. 37761

01 INFORMATION DISCLOSURE CITATION
IN AN APPLICATION

MAY 06 2004

(to several sheets if necessary)

Docket Number (Optional)

TSMC-03-627

Application Number

10/807,081

Applicant

Hung-Wei Chen et al.

Filing Date

03/23/04

Drawn At Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	TITLE	CLASS	SUBCLASS	PLUG DATE IF APPROPRIATE
	5468657	11/21/95	Hsu	437	24	6/17/94
	6613678	9/2/03	Sakaguchi et al.	438	695	5/17/99
	6410938	6/25/02	Xiang	257	49	4/3/01
	5656537	8/12/97	Iwamatsu et al.	438	402	6/5/95
	5910672	6/8/99	Iwamatsu et al.	257	347	7/7/97

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Portmox Pages, Etc.)

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.